

SPECIALITY: COMPUTER ENGINEERING

OPTION: DATABASE MANAGEMENT

EXAM PAPER: DIGITAL ELECTRONICS

CODE: DBM 19

CREDIT VALUE: 7

DURATION: 3 HOURS

NATURE OF EXAM: WRITTEN

Answer all questions. Orderly presentation of your work is necessary. No programmable or pictured instrument is allowed.

SECTION A: NUMBER SYSTEMS AND CODES

20 mark

9) In Excess-3 code each coded number is.....than in BCD code.

- (a) four larger
 - (b) three smaller
 - (c) three larger
 - (d) much larger.

10) which numbering system uses numbers and letters as symbols

- (a) decimal
 - (b) binary
 - (c) Octal
 - (d) hexadecimal

11) To convert a whole decimal number into a hexadecimal equivalent, one should divide the decimal value by.....

- (a) 2
 - (b) 8
 - (c) 10
 - (d) 16

12) The number 12_8 is equivalent to decimal

13) The result of binary multiplication $111_2 \times 10_2$ gives

14) -8 is equal to signed binary number

15) Digital system is usually operated on.....system

- a) Binary b) decimal c) Octal d) hexadecimal

16) What is the binary equivalent of the decimal number 368

- (A) 101110000 (B) 110110000
(C) 111010000 (D) 111100000

17) The decimal equivalent of hex number 1A53 is

18) The hexadecimal number ‘A0’ has the decimal value equivalent to

(A) 80

(B) 256

(C) 100

(D) 160

19) The Gray code for decimal number 6 is equivalent to

(A) 1100

(B) 1001

(C) 0101

(D) 0110

20) The binary system uses powers of for position values

a) 2 b) 10 c) 8 d) 16

SECTION B: COMBINATIONAL LOGIC

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EXERCISE I

Simplify the Boolean function below using the Boolean algebra method

$$F(x,y,z) = \bar{x}yz + \bar{x}y\bar{z} + xz$$

1. FULL ADDER

- a) Draw the block diagram of a full adder
- b) Draw the truth table considering A, B and C_{in} as the inputs
- c) Bring out the output logic equations from the truth table
- d) Draw the logic circuit

2. MULTIPLEXER

Use an 8 – to – 1-line multiplexer to implement the Boolean expression

$$f(A, B, C) = \bar{A} \cdot B \cdot \bar{C} + A \cdot \bar{B} \cdot \bar{C} + A \cdot B \cdot C$$

SECTION C: SEQUENTIAL LOGIC

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EXERCISE 1

1. Draw the waveform of the output Q of clocked R S flip-flop, if R and S

inputs applied to it, are as represented. The latch is initially reset

EXERCISE 2

2. Modify an asynchronous R S flip-flop so that when both the inputs R and S are 1, the flip-flop is set.